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1 Overview

A not-quite-ready footprint reference that contains footprint design guidelines, dimensioned drawings of footprints and embedded manufacturer datasheets.

1.1 Objectives

1. To provide footprint design guidelines to be used in the design of footprints.
2. To provide footprint reference information to be used in the design of printed circuit boards (PCBs).

Question, comments, observations, unmarked bills to jluciani at gmail dot com

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2 Design Guidelines

These are the design guidelines I use to create footprints. Most of the footprints I have created should meet these guidelines. As older footprints are updated I will make the necessary corrections. *These guidelines will evolve closer to IPC-7351 (after I get my copy).*

Figure 1 contains size specifications for copper, silkscreen, clearances and finished holes. These sizes seem consistent with most of the low-cost PCB houses. These sizes are decreasing as package sizes decrease and as the low-cost PCB houses improve their processes.

Parameter	Min	Typ.	Max	units	Notes
Silkscreen					
width	10			mils	
spacing	10			mils	
Copper					
width	7	8		mils	
annular ring	8	10		mils	
Clearance					
copper	7	8		mils	
mask	10			mils	
Finished Hole Sizes					
See the finished-hole size table					

Figure 1: Design Specifications

Copper

The copper widths and spacing are defined in Figure 1 and are consistent with the capabilities of low-cost PCB houses. All of the footprints that I have created will meet a `7/7 mil`. The annular ring specification is from PCB Express.

The pad dimensions I use are specified in the manufacturer's datasheets.

Silkscreen

The silkscreen line widths and spacing are defined in Figure 1 and are consistent with the capabilities of low-cost PCB houses.

body outline The silkscreen that defines the body of the component is kept within the body outline. Except for the smallest components I try to make the silkscreen outline mimic the body outline. If the body is too narrow I will use a single line.

pin markings Polarity and pin one markings are kept outside the body outline. Pin one marking is typically a dot but if the manufacturer has a pin one body feature I will add a similar silkscreen feature (space permitting).

mounting holes I place a silkscreen circle around mounting holes for increased visibility. I will draw additional silkscreen to represent preferred mounting hardware (*e.g.* washer and hex nut).

Orientation

origin of part I try to make this the centroid. A few of my parts have pin one as the origin but these will be changed.

rotation of part The placement preferences for pin one are — (1) upper left for parts with pin one in a corner, (2) top for parts with pin one not in a corner and (3) left for parts with two pins. However, if the manufacturer has a component footptrint drawing I usually use the orientation in that drawing. A side-by-side comparison is easier when both footprints have the same orientation. *For future parts I will probably switch to a fixed rotation regardless of the manufacturer drawing.*

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pin one

diodes Cathode is pin one.

polarized two-terminal devices Positive terminal.

Manufacturing Data

courtyard Nothing implemented yet.

revision control Nothing implemented yet.

material condition Material condition usually follows the manufacturer's datasheet. I do not know if these are most, nominal or least condition. *Depending on the definitions of most, nominal and least in IPC-7351 I may add a material condition larger than most that is useful for assembly and repair by novices.*

part numbers See the specification `http://www.luciani.org/geda/pcb/footprint-name-spec.pdf`

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2.1 Finished Hole Sizes

The finished-hole size table groups the finished hole sizes of two PCB vendors, PCB Express and AP Circuits. The `Size` column is the value that is specified in the drill file to get the size defined in `Finished Hole Size` column. All measurements are in mils.

The finished hole size specifications are quite different for these two manufacturers. PCB Express specifies a ±4mil tolerance finished hole size while AP circuits specifies a drill size (no tolerance) and a plating reduction of 3-5mils. I do not know why one vendor has an 8mil specification and the other has a 2mil specification.

To pick a hole size I try to find a size that is common between both vendors (if possible) that passes one of the following rules:

(1) If the manufacturer specifies a lead diameter I choose a finished hole size that is ($\frac{+12}{+5}$mils) larger than a maximum specification or ($\frac{+15}{+5}$mils) larger than a typical specification.

(2) If the manufacturer specifies a finished hole specification] finished hole size that is within ($\frac{+2}{-5}$mils) for a maximum specification or within (±5mils) for a typical specification.

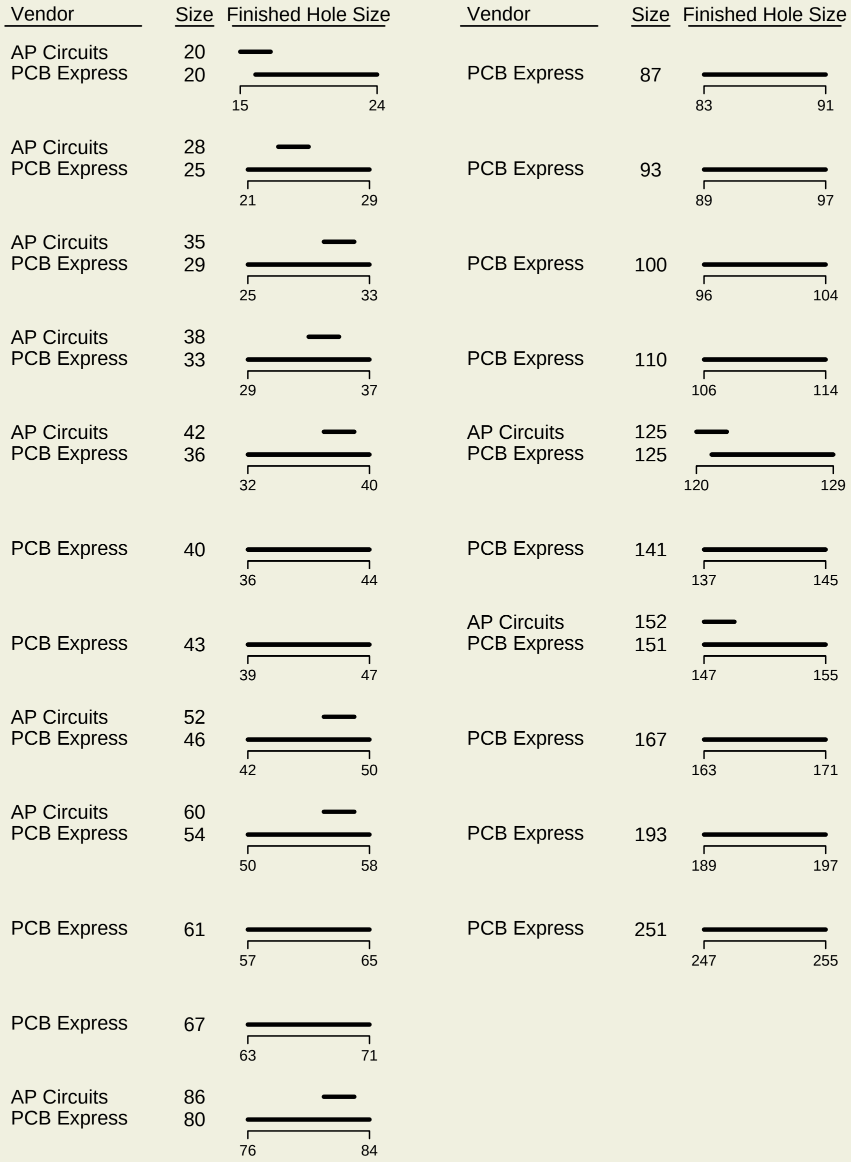

Figure 2: Finished Hole Sizes

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3 `pkg2mp` and `fpl2tex`

`pkg2mp` is used to create a dimensioned drawing of a footprint using the data contained in the footprint file. The footprint file is parsed (Perl) and the various METAPOST commands are written. The output from METAPOST is converted to a pdf file.

The script `fpl2tex` creates this document by merging the dimensioned drawings and manufacturer datasheets, prepending a LaTeX file and creating the various hyperlinks and hypertargets.

Many open issues (in no particular order) —

1. Add dimension notes and scale label to the drawing.
2. Group similar components and dimension a single representative sample. Don't really need to show 20 Molex 8624 headers that only differ by pin count and length. Pick the one with the median number of pins and dimension it with reference letters and add a dimension table.
3. Add dimension lines for the component body and mounting holes.
4. Correct the extension lines.
5. Display pin numbers.
6. Add staggered numerals for the dimension lines.
7. Create a table that lists the footprint specifications — pins, pads, holes, *etc.*
8. Add configuration file options to support dimensioning hints for unusual parts.
9. Add configuration file option to skip dimensioning for the very unusual parts.
10. Evaluate placing a scaled-down version of the datasheet next to the footprint. The datasheet could be hyperlinked to a fullpage version.
11. Cleanup the boundingbox algorithm that places the dimension lines.
12. Cleanup the finished hole page. Add title, units, typesetting, *etc.*

3.1 Configuration File

Listing 1: Configuration File for `pkg2mp`

```
# Configuration file for the pkg2mp program (probably should be called fp2mp)

# definitions start with @def@
# comments start with # and end at the newline
# line continuation if the last non-whitespace character on a line is
# a backslash
# any line containing a non-whitespace character that is not a comment
# or a definition is a datarecord except for the lines after __END__
# which are discarded.

# datasheet_dir    the name of the directory containing the datasheets
```

```
# footprint_dir   the name of the directory containing the footprints
# fields          the names of the fields for each data record contained in this file
#   regex         just a file glob for now. Will be a Perl regex (or an SQL pattern)
#   label_units   the units to use for dimension labels. This will be eliminated if
#                 units are written as mm over inches.
#   datasheet     datasheet filename (only pdf files for now). Will add options
#                 for http:// and file://
#   pages         the pages of the datasheet to include

@def@ datasheet_dir /local/pub/datasheets/
@def@ footprint_dir /local/lan/pcb/packages/
@def@ fields regex label_units datasheet pages

# regex                                    | units| datasheet                              | pages

DIP-48-600                                 | mils | Texas-Instruments/mpdi008.pdf          | 1
CON_HDR-200P-10C-1R-10N__JST_B10B-PH-K     | mm   | JST/PH-series-connectors-ePH.pdf       | 3
CON_HDR-254P-10C-2R-20N__Molex_8624-Series | mils | Molex/dual-row-vertical-header-8624.pdf | 1
TSSOP-65P-640L1-16N                        | mm   | Texas-Instruments/max3221.pdf          | 12

__END__

DIP-*-300                                  | mils | Texas-Instruments/mpdi002c.pdf         | 1
DIP-*-600                                  | mils | Texas-Instruments/mpdi008.pdf          | 1
*__Molex_8624-Series                       | mils | Molex/dual-row-vertical-header-8624.pdf | 1
```

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References

Brorson, S. D., & Meier, S. (2005, January). Footprint creation for the open-source layout program PCB. (Retrieved February 6, 2005, from http://www.brorson.com/gEDA/land_patterns_20050129.pdf)

Eaton, H., & Nau, T. (2002). Pcb [Computer software and manual]. (Retrieved February 6, 2005 from http://pcb.sourceforge.net/pcb-20050127.html/index.html)

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Hobby, J. D. (1992). *A User's Manual for MetaPost* (Tech. Rep. No. no. 162). Murray Hill, New Jersey: AT&T Bell Laboratories. (Retrieved Nov 26, 2005, from http://cm.bell-labs.com/who/hobby/cstr_162.pdf

IPC. (2005, January). IPC-7351 Naming Convention for Standard SMT Land Patterns. (Retrieved July 7, 2005, from http://landpatterns.ipc.org/IPC-7351Table3-15January2005.pdf)

Knuth, D. E. (1986). *The METAFONTbook* (Vol. C). Reading, MA, USA: Addison-Wesley.

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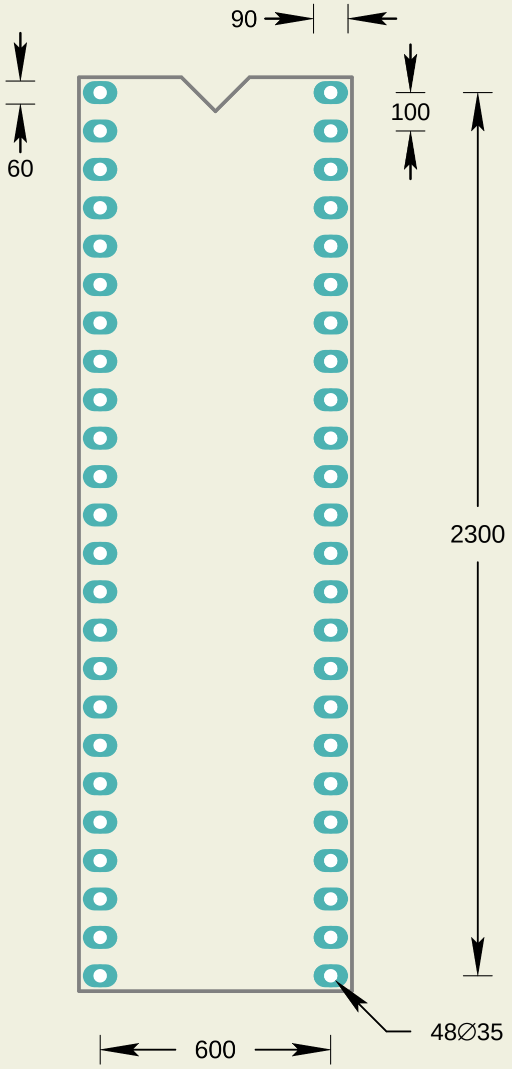
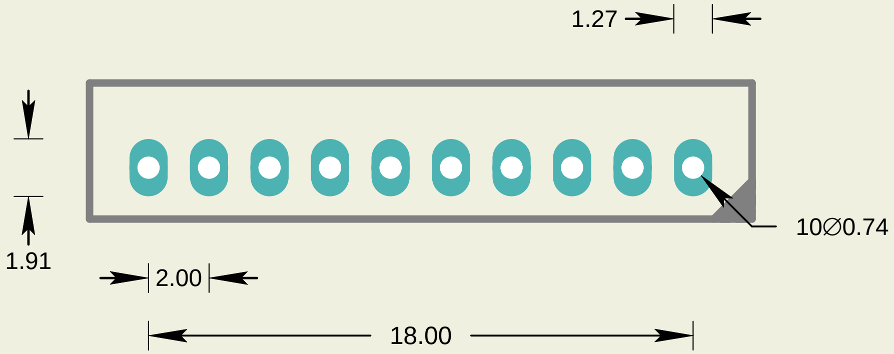
DIP-48-600

DATASHEET



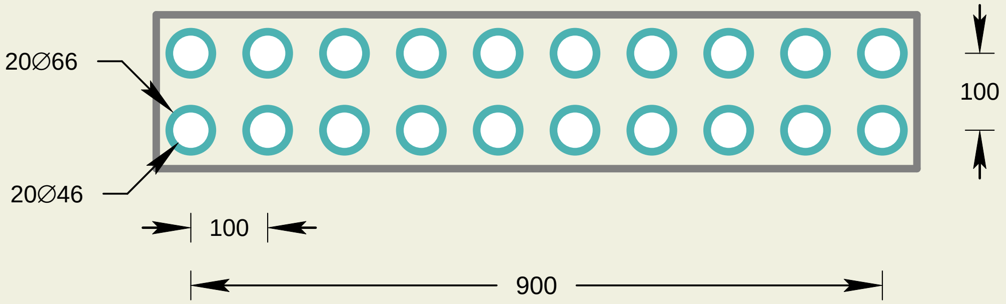
CON_HDR-200P-10C-1R-10N__JST_B10B-PH-K

DATASHEET



CON_HDR-254P-10C-2R-20N__Molex_8624-Series

DATASHEET



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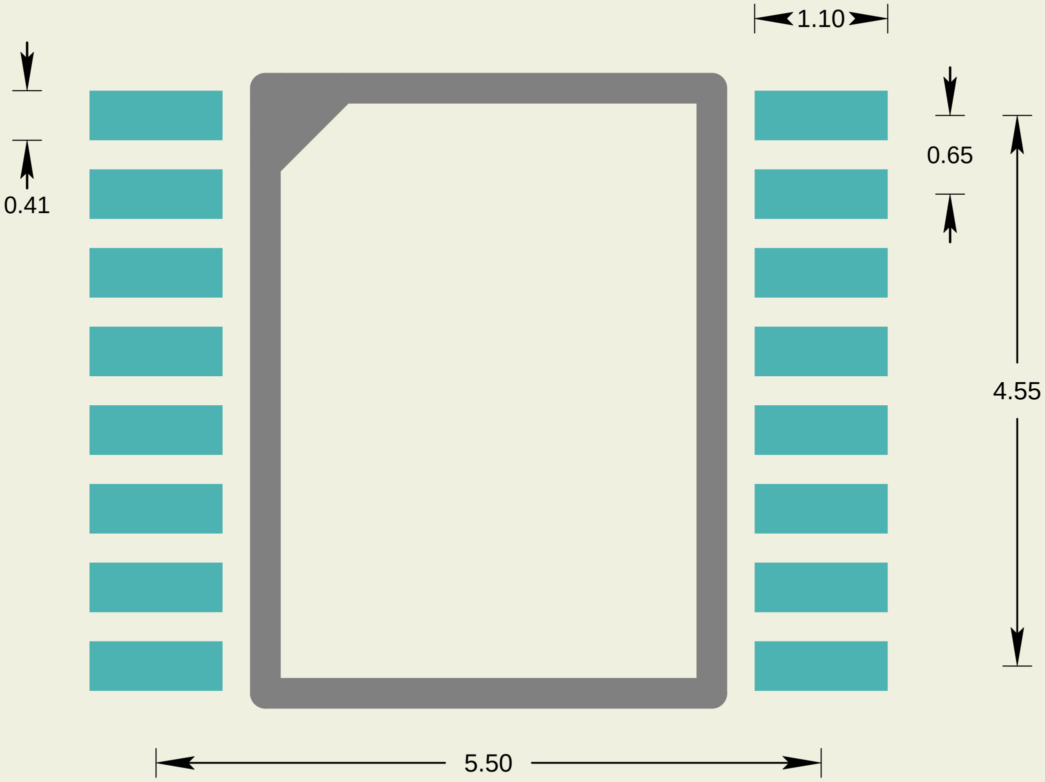
TSSOP-65P-640L1-16N

DATASHEET



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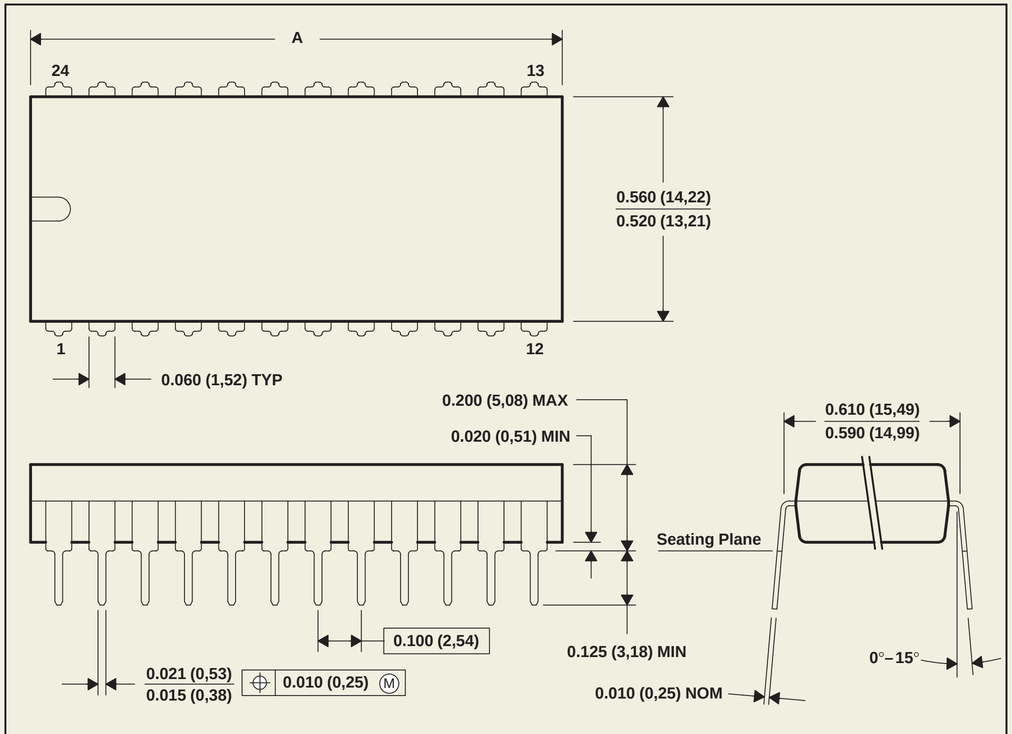
N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

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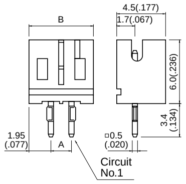
Through-hole type shrouded header

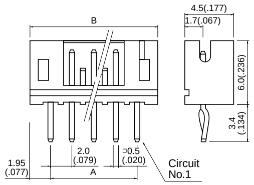
The shrouded headers are interchangeable with those of the KR, KRD and CR insulation displacement connectors.

Top entry type

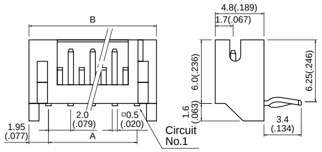
(2 circuits)



(3 circuits or more)



Side entry type



Cir-cuits	Model No.		Dimensions mm(in.)		Q'ty / box	
	Top entry type	Side entry type	A	B	Top entry type	Side entry type
2	**B 2B-PH-K-S**	**S 2B-PH-K-S**	2.0(.079)	5.9(.232)	1,000	1,000
3	**B 3B-PH-K-S**	**S 3B-PH-K-S**	4.0(.157)	7.9(.311)	1,000	1,000
4	**B 4B-PH-K-S**	**S 4B-PH-K-S**	6.0(.236)	9.9(.390)	1,000	500
5	**B 5B-PH-K-S**	**S 5B-PH-K-S**	8.0(.315)	11.9(.469)	1,000	500
6	**B 6B-PH-K-S**	**S 6B-PH-K-S**	10.0(.394)	13.9(.547)	1,000	500
7	**B 7B-PH-K-S**	**S 7B-PH-K-S**	12.0(.472)	15.9(.626)	500	500
8	**B 8B-PH-K-S**	**S 8B-PH-K-S**	14.0(.551)	17.9(.705)	500	250
9	**B 9B-PH-K-S**	**S 9B-PH-K-S**	16.0(.630)	19.9(.783)	500	250
10	**B10B-PH-K-S**	**S10B-PH-K-S**	18.0(.709)	21.9(.862)	500	250
11	**B11B-PH-K-S**	**S11B-PH-K-S**	20.0(.787)	23.9(.941)	500	250
12	**B12B-PH-K-S**	**S12B-PH-K-S**	22.0(.866)	25.9(1.020)	500	250
13	**B13B-PH-K-S**	**S13B-PH-K-S**	24.0(.945)	27.9(1.098)	250	250
14	**B14B-PH-K-S**	**S14B-PH-K-S**	26.0(1.024)	29.9(1.177)	250	250
15	**B15B-PH-K-S**	**S15B-PH-K-S**	28.0(1.102)	31.9(1.256)	250	200
16	**B16B-PH-K-S**	**S16B-PH-K-S**	30.0(1.181)	33.9(1.335)	250	200

Material and Finish
Post: Brass, copper-undercoated, tin/lead-plated Wafer: Nylon 66, UL94V-0, natural (white)

<For reference> As the color identification,
the following alphabet shall be put in the underlined part.
For availability, delivery and minimum order quantity, contact JST.

ex. **B2B-PH-K-oo**

S…natural (white)
BK…black R…red TR…tomato red
E…blue Y…yellow L…lemon yellow M…green
D…orange N…brown P…purple PK…pink H…gray
LE…light blue FY…vivid yellow (blank)…ivory

Component Groups
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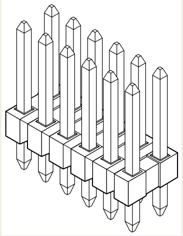
CON_HDR
TSSOP

2.54mm (.100") Pitch C-Grid® Breakaway Header

8624

Dual Row, Vertical



FEATURES AND SPECIFICATIONS

Features and Benefits

- Sizes 4 to 80 circuits
- Stackable side-to-side and end-to-end (on unbroken edges)
- Easy breakaway to smaller sizes
- Drawn .025" square wire provides 4-sided smooth surface for quality interface
- For high temperature version contact factory, engineering series 70280

Reference Information

Product Specification: PS-8624
Packaging: Bag
UL File No.: E29179 (G)
CSA File No.: LR19980A
Mates With: 7859 Shunts, C-Grid Receptacles, MX50 Connectors, SL Crimp and IDT Housings
Designed In: Inches

Electrical

Voltage: 250V
Current: 3.0A
Contact Resistance: 15mΩ max.
Dielectric Withstanding Voltage: 600V
Insulation Resistance: 1000 MΩ min.

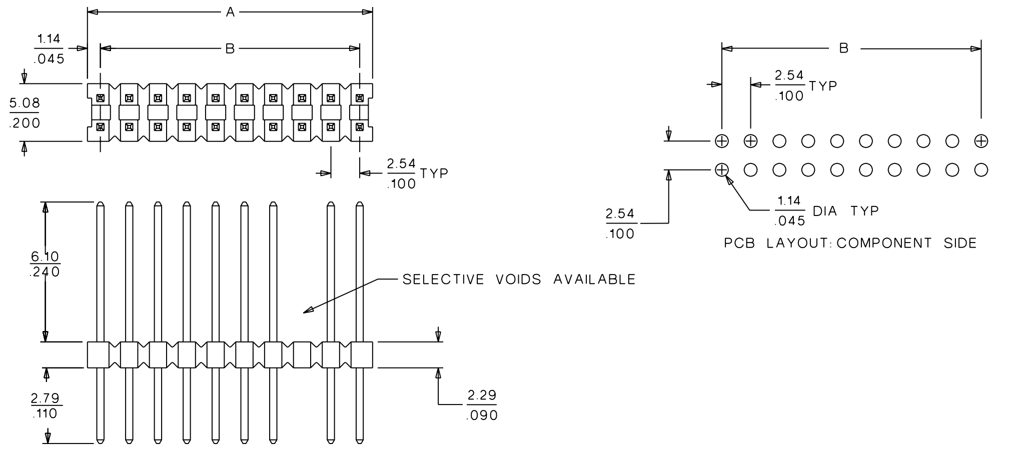
Mechanical

Pin Retention to Header: 1.8kg (4 lb)
Durability: 25 cycles Tin/Lead and 50 cycles Gold

Physical

Housing: Glass-filled polyester, UL 94V-0
Contact: Phosphor Bronze
Plating: See Table
Temperature: -40 to +105˚C

Not For Use With Molex C-Grid III™ Components



ORDERING INFORMATION AND DIMENSIONS

Circuits	Dimension	
	A	B
4	4.83 (.190)	2.54 (.100)
6	7.37 (.290)	5.08 (.200)
8	9.91 (.390)	7.62 (.300)
10	12.45 (.490)	10.16 (.400)
12	14.99 (.590)	12.70 (.500)
14	17.53 (.690)	15.24 (.600)
16	20.07 (.790)	17.78 (.700)
18	22.61 (.890)	20.32 (.800)
20	25.15 (.990)	22.86 (.900)
22	27.69 (1.090)	25.40 (1.000)
24	30.23 (1.190)	27.94 (1.100)
26	32.77 (1.290)	30.48 (1.200)
28	35.31 (1.390)	33.02 (1.300)

Circuits	Dimension	
	A	B
30	37.85 (1.490)	35.56 (1.400)
32	40.39 (1.590)	38.10 (1.500)
34	42.93 (1.690)	40.64 (1.600)
36	45.47 (1.790)	43.18 (1.700)
38	48.01 (1.890)	45.72 (1.800)
40	50.55 (1.990)	48.26 (1.900)
42	53.09 (2.090)	50.80 (2.000)
44	55.63 (2.190)	53.34 (2.100)
46	58.17 (2.290)	55.88 (2.200)
48	60.71 (2.390)	58.42 (2.300)
50	63.25 (2.490)	60.96 (2.400)
52	65.79 (2.590)	63.50 (2.500)
54	68.33 (2.690)	66.04 (2.600)

Circuits	Dimension	
	A	B
56	70.87 (2.790)	68.58 (2.700)
58	73.41 (2.890)	71.12 (2.800)
60	75.95 (2.990)	73.66 (2.900)
62	78.49 (3.090)	76.20 (3.000)
64	81.03 (3.190)	78.74 (3.100)
66	83.57 (3.290)	81.28 (3.200)
68	86.11 (3.390)	83.82 (3.300)
70	88.65 (3.490)	86.36 (3.400)
72	91.19 (3.590)	88.90 (3.500)
74	93.73 (3.690)	91.44 (3.600)
76	96.27 (3.790)	93.98 (3.700)
78	98.81 (3.890)	96.52 (3.800)
80	101.35 (3.990)	99.06 (3.900)

Plating Option	Order No.
15µ" min. select Gold	• 10-89-1XX1
30µ" min. select Gold	• 10-89-2XX1
150µ" Tin/Lead, Nickel overall	• 10-88-1XX1
5µ" min. Gold flash	• 10-89-9XX7
Replace XX with no. of circuits, 04-80 (even only), for 2-circuit, see 42375	

• US Standard Product, available through Molex franchised distributors

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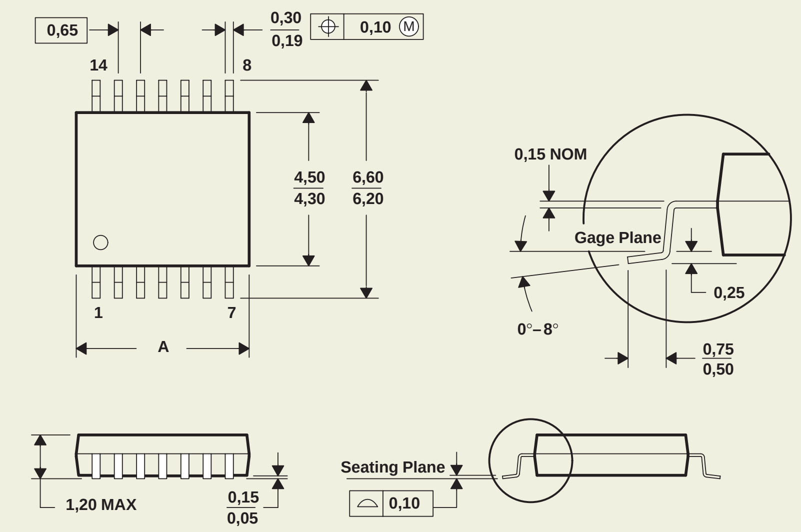
PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

Component Groups

DIP
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DIP

DIP-48-600

CON_HDR

CON_HDR-200P-10C-1R-10N__JST_B10B-PH-K
CON_HDR-254P-10C-2R-20N__Molex_8624-Series

TSSOP

TSSOP-65P-640L1-16N

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